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In re Patent Application of:
MARINET ET AL.

Serial No. **NOT YET ASSIGNED**

Filing Date: **HEREWITH**

For: **METHOD AND DEVICE FOR PROTECTING INTEGRATED CIRCUITS AGAINST PIRACY**

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 15.

Please add new Claims 16 to 45.

16. A method of protecting an integrated circuit against piracy comprising:

detecting the state of at least one timer before a predetermined processing sequence performed by the integrated circuit;

activating the timer if it is not activated; and

disabling the integrated circuit if the timer is activated.

17. A method according to Claim 16, further comprising deactivating the timer if the predetermined processing sequence has been performed by the integrated circuit.

18. A method according to Claim 16, further comprising:

modifying the value of a counter within a protected area in a non-volatile memory if it is detected that the timer is activated;

comparing the counted value with a predefined threshold; and

performing a process for protecting confidential data stored within memories in the integrated circuit if the counted value reaches the predefined threshold.

19. A method according to Claim 18, wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit.

20. A method according to Claim 18, wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit.

21. A method according to Claim 18, wherein the protection process comprises erasing all memories in the integrated circuit.

22. A method according to Claim 16, wherein the at least one timer comprises a plurality of timers each being

associated with a respective authentication calculation of a sequence of a predefined number of calculations; and further comprising:

detecting the state of a respective timer before performing an associated calculation,

activating the respective timer if it is not activated; and

disabling the integrated circuit if the respective timer is activated.

23. A method of protecting an integrated circuit (IC) against tampering, the IC having a central processing unit (CPU), the method comprising:

providing at least one timer associated with the CPU;

detecting a state of the at least one timer before beginning an operating session of the integrated circuit;

activating the timer if it is not activated; and

disabling the integrated circuit if the timer is activated.

24. A method according to Claim 23, further comprising deactivating the timer if the operating session is performed by the integrated circuit.

25. A method according to Claim 23, further comprising:

modifying the value of a counter within a protected area in a non-volatile memory if it is detected that the timer is activated;

comparing the counted value with a predefined threshold; and

performing a process for protecting confidential data stored within memories in the integrated circuit if the counted value reaches the predefined threshold.

26. A method according to Claim 25, wherein the protection process comprises erasing the confidential data from the memories in the integrated circuit.

27. A method according to Claim 25, wherein the protection process comprises erasing a secret code stored within a memory in the integrated circuit.

28. A method according to Claim 25, wherein the protection process comprises erasing all memories in the integrated circuit.

29. A method according to Claim 23, wherein the at least one timer comprises a plurality of timers each being associated with a respective authentication calculation of a sequence of a predefined number of calculations; and further comprising:

detecting the state of a respective timer before performing an associated calculation,

activating the respective timer if it is not activated; and

disabling the integrated circuit if the respective timer is activated.

30. An integrated circuit protected against piracy, comprising:

at least one timer circuit comprising

a timer designed to remain in an activated state as long as the circuit is powered-on and for a predetermined duration if the circuit is powered-off,

means for activating the timer,

means for deactivating the timer, and

means for detecting the activated or deactivated state of the timer; and

means for reading the timer state, and for disabling the integrated circuit at predefined times if the timer is in the activated state.

31. An integrated circuit according to Claim 30, wherein the deactivating means deactivates the timer after normal execution of a predetermined processing sequence.

32. An integrated circuit according to Claim 30, wherein each timer circuit further comprises:

means for detecting a power supply; and

means for allowing the timer to be activated or deactivated when the power supply is detected during a predetermined time period.

33. An integrated circuit according to Claim 30, wherein the at least one timer circuit comprises a plurality of timer circuits, each timer circuit being associated with an authentication calculation performed by the integrated

circuit; and further comprising means for determining, before each calculation, the state of the timer associated with the calculation, activating the associated timer if it is not activated, and disabling the integrated circuit if the associated timer is activated.

34. An integrated circuit according to Claim 30, wherein the at least one timer circuit comprises:

a capacitor;

a discharge circuit associated with the capacitor and designed so that the capacitor slowly discharges when the device is powered-off;

a circuit for detecting capacitor charging;

means for controlling capacitor charging; and

means for controlling capacitor discharging.

35. An integrated circuit according to Claim 34, wherein the means for controlling capacitor discharging is designed for discharging the capacitor more rapidly than when the device is powered-off.

36. An integrated circuit according to Claim 34, wherein the at least one timer circuit further comprises a MOS transistor associated with the capacitor so that it is only discharged by a leakage current when the integrated circuit is powered-off.

37. An integrated circuit according to Claim 30, further comprising a test circuit for reducing the

predetermined duration of the timer during a testing procedure.

38. An integrated circuit (IC) comprising:

a central processing unit (CPU);

at least one timer circuit for protecting the IC against piracy and comprising

a timer which is activated when the IC is powered-on and for a predetermined duration when the IC is powered-off,

a timer activating circuit for activating the timer,

a timer deactivating circuit for deactivating the timer, and

a detection circuit for detecting the state of the timer; and

an IC disabling circuit for disabling the IC at predefined times if the timer is in the activated state.

39. An integrated circuit according to Claim 38, wherein the deactivating circuit deactivates the timer after normal execution of a predetermined processing sequence.

40. An integrated circuit according to Claim 38, wherein each timer circuit further comprises:

a power supply detection circuit for detecting a power supply; and

a timer control device for allowing the timer to be activated or deactivated when the power supply is detected during a predetermined time period.

41. An integrated circuit according to Claim 38, wherein the at least one timer circuit comprises a plurality of timer circuits each being associated with an authentication calculation performed by the IC.

42. An integrated circuit according to Claim 38, wherein the at least one timer circuit comprises:

a capacitor;

a discharge circuit associated with the capacitor and designed to discharge over the predetermined duration when the IC is powered-off;

a circuit for detecting capacitor charging;

a capacitor charging control circuit; and

a capacitor discharging control circuit.

43. An integrated circuit according to Claim 42, wherein the capacitor discharging control circuit discharges the capacitor faster than when the IC is powered-off.

44. An integrated circuit according to Claim 42, wherein the at least one timer circuit further comprises a MOS transistor associated with the capacitor so that it is only discharged by a leakage current when the IC is powered-off.

45. An integrated circuit according to Claim 38, further comprising a test circuit for reducing the predetermined duration of the timer during a testing procedure.

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Serial No. **Not Yet Assigned**
Filing Date: **Herewith**

REMARKS

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination, a Notice of Allowance is respectfully requested in due course. If any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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